In the Claims:

1. (Currently Amended) A method for increasing the size of a portion of main trench structures ~~below a selected depth beneath the surface~~ of a semiconductor ~~substrate,~~component, said portion of each main trench structure having sidewalls and is to be formed in a depth under the surface of a semiconductor substrate, said method comprising:

providing [[a]] said semiconductor substrate comprising a crystalline material with a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are less resistant to etching;

~~forming said main structures having sidewalls~~ arranging at the surface of [[in]] the semiconductor substrate ~~in checkered fashion in~~ first areas of a rectangular surface grid, said first areas being provided in checkered fashion for forming said main trench structures and alternating with second areas ~~at a surface of the semiconductor substrate, said first areas~~ of said rectangular surface ~~grid alternating with second areas of said~~ grid, said second areas being provided for forming secondary structures in a section of the semiconductor substrate that is near said surface thereof;

setting x, y axes of the surface grid to be parallel to the crystal faces that are less resistant to etching; and

etching said sidewalls of said portion of the formed main trench structures ~~to increase the size of the main structures below said selected~~ in a depth under said surface of ~~such that sections of the main trench structures formed in~~ said semiconductor substrate to expand said sidewalls to beneath ~~extend below~~ said second areas of said surface grid.

2. (Previously Presented) The method of claim 21, wherein a large structure having the main structures is imaged onto the surface of the semiconductor substrate by means of an exposure device with the x, y axes of the surface grid parallel to the crystal faces of the semiconductor substrate that are less resistant to etching.

3. (Currently Amended) The method of claim 2, wherein prior to imaging, a mask having [[a]] ~~rectangularly patterned~~ rectangular mask openings in a layout of the large structure is oriented in accordance with the crystal faces of the semiconductor substrate that are less resistant to etching.

4. (Currently Amended) The method of claim 21, wherein a semiconductor wafer is provided as the semiconductor substrate and a marking identifying a crystal orientation of the crystal lattice is provided at ~~and/or on~~ the semiconductor wafer.

5. (Original) The method of claim 4, wherein a crystal orientation identifying the orientation of the crystal faces that are less resistant to etching is identified by the marking.

6. (Original) The method of claim 5, wherein the marking is used for the orientation of a mask in an exposure device.

7. (Currently Amended) The method of claim 21, further comprising providing the main trench structures at the surface of the semiconductor substrate with an oval cross section.

8. (Previously Presented) The method of claim 21, wherein monocrystalline silicon is provided as the material of the semiconductor substrate.

9. (Original) The method of claim 8, wherein the surface grid is oriented in accordance with a <100> crystal orientation of the monocrystalline silicon.

10. (Currently Amended) The method of claim 9, wherein during the ~~area-selective~~ etching process, the <100> crystal faces having a lower etching resistance are etched more rapidly than the <110> crystal faces that are more resistant to etching.

11. (Currently Amended) The method of claim 21, wherein upper sections of the main trench structures, between the surface of the semiconductor substrate and at least one lower edge of the secondary structures, are provided with a protective layer that is resistant to the etching process expanding ~~etching process for increasing the size~~ said sidewalls of said main trench structure.

12. (Previously Presented) The method of claim 21, wherein the main trench structures are functionally designed as storage capacitances.

13. (Previously Presented) The method of claim 21, wherein the secondary structures are selection transistors formed in the second areas for use with the storage capacitances of DRAM cells.

14-20. (Canceled)

21. (Currently Amended) A method for increasing a structure size of main trench structures in a depth under a surface of [[in]] a semiconductor substrate, said method comprising:

providing [[a]] said semiconductor substrate comprising a crystalline material with a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are

less resistant to etching;

arranging first areas for forming said main trench structures ~~on the semiconductor substrate~~ in checkered fashion in a rectangular surface grid, at a surface of the semiconductor substrate, ~~in each case in alternation with secondary structures formed in each case~~ said first areas respectively alternating with second areas for respectively alternating with a second areas for respectively forming secondary structures substantially in a section of the semiconductor substrate that is near a surface thereof;

setting x, y axes of the surface grid to be parallel to the crystal faces that are less resistant to etching; and

performing area-selective etching to increase the structure size of the main trench structures in said depth under said semiconductor substrate's surface so that the structure size increased main trench structures are expanded to beneath sections of said secondary ~~such that sections of the semiconductor substrate, which are located below secondary structures are made available for the formation of extended main~~ structures.

22. (Currently Amended) The method of claim 1, wherein a large structure having the main trench structures [[are]] is imaged onto the surface of the semiconductor substrate by means of an exposure device with the x, y axes of the surface grid parallel to the crystal faces of the semiconductor substrate that are less resistant to etching.

23. (Currently Amended) The method of claim 22, wherein prior to said imaging, a mask having [[a]] ~~rectangularly~~ rectangular ~~patterned~~ mask openings in a layout of the large structure is oriented in accordance with the crystal faces of the semiconductor substrate that are less resistant to etching.

24. (Currently Amended) The method of claim 1, wherein a semiconductor wafer is provided as the semiconductor substrate and a marking identifying a crystal orientation of the crystal lattice is provided at [[or on]] the semiconductor wafer.

25. (Previously Presented) The method of claim 24, wherein said crystal orientation represents the orientation of the crystal faces that are less resistant to etching is identified by the marking.

26. (Previously Presented) The method of claim 25, wherein said marking is used for orienting a patterned mask.

27. (Currently Amended) The method of claim 1, further comprising providing the main ~~trench~~ structures at the surface of the semiconductor substrate with an oval cross section.